IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously amended) A method for performing a high stress built-in self-repair for a memory, comprising the operations of:

providing an internal clock signal for use in accessing a memory array, the memory array having access to redundant memory cells during normal operation;

performing a built-in self-test on the memory array at each ~~power-on~~ power-up event using a stress clock signal, wherein the stress clock signal has a predetermined frequency greater than the internal clock signal, the predetermined frequency simulating functioning of the memory array under stressed environmental and operating conditions, and wherein the stress clock signal is not used during normal memory access operations;

storing defective memory addresses detected by the built-in self-test in a memory block; and

redirecting memory access operations to the defective memory addresses to redundant memory cells.

2. (original) A method as recited in claim 1, wherein the memory block is a register.

3. (original) A method as recited in claim 1, wherein the internal clock signal is based on required read and write times for memory cells of the memory array.

4. (original) A method as recited in claim 3, wherein the internal clock signal is further based on a margin added to the required read and write times for memory cells of the memory array.

5. (original) A method as recited in claim 4, wherein an amount of optimal margin is derived from expected variations in required read and write times for the memory cells of the memory array due to possible variations in environmental conditions and operating conditions.

6. (cancelled)

7. (cancelled)

8. (Previously amended) A method as recited in claim 5, wherein the internal clock signal is used during normal memory access operations.

9-12 (Cancelled).

13. (Cancelled)

14-21. (Cancelled)

22.-23. (cancelled)